PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2000-058695
(43)Date of publication of application : 25.02.2000

(51)Int.Cl. H01L 23/12

(21)Application number : 10-221559
(22)Date of filing : 05.08.1998

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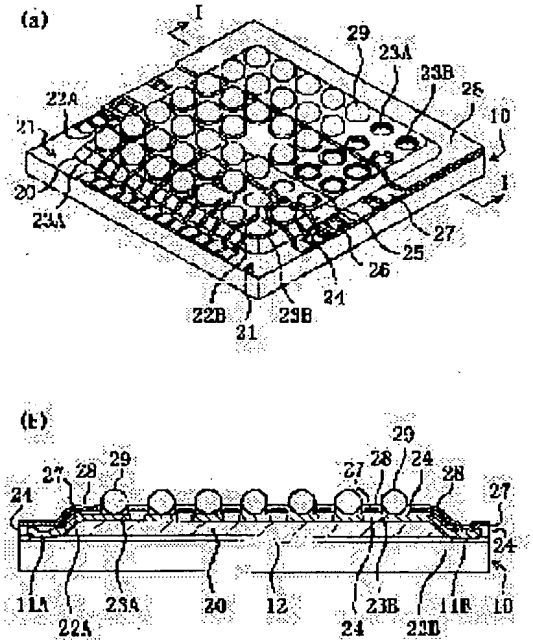
(54) SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

(57)Abstract:
PROBLEM TO BE SOLVED: To realize a semiconductor device with a chop that is hardly effected by external noise components and has little spurious radiations from the semiconductor chip itself.
SOLUTION: On the main surface of a semiconductor chip 10 are provided a first insulation layer 20 having a usual electrode 11A and reference potential electrode 11B exposed on the surface, metal wirings 22A, 22B which extend from the usual electrode 11A and reference potential electrode 11B and are connected to lands 23A, 23B on the first insulation layer 20, second insulation layer 24 with the metal wiring 22B and lands 23A, 23B exposed on the reference positional electrode 11B, a shield metal layer 27 which is formed on the second insulation layer 24 and electrically connected to the metal wiring 22B on the reference potential electrode 11B, solder resist 28 formed with the lands 23A, 23B exposed, and metal balls 20. In this constitution, the shield metal layer 27 having a potential equal to the reference potential of the semiconductor chip 10 suppresses the effects of noise components and spurious radiations from the semiconductor chip 10.



LEGAL STATUS

[Date of request for examination] 27.09.2001
[Date of sending the examiner's decision of rejection]
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]
[Date of final disposal for application]
[Patent number] 3477375
[Date of registration] 26.09.2003

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

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CLAIMS

[Claim(s)]

[Claim 1] The semiconductor chip with which the reference potential electrode connected with an electrode on a principal plane at a reference potential has been arranged, The 1st insulating layer to which it was prepared on said principal plane, and opening of the part corresponding to the upper part of said electrode and the part corresponding to the upper part of said reference potential electrode was carried out respectively, Wiring which was connected to said electrode through opening of said 1st insulating layer, and extended to up to said 1st insulating layer, The external electrode terminal for connecting with said wiring, being prepared on said 1st insulating layer, and delivering and receiving a signal between external instruments, The 2nd insulating layer to which opening of the part corresponding to the upper part of said reference potential electrode and the part corresponding to the upper part of said external electrode terminal was respectively carried out with the wrap in said electrode and said wiring, The semiconductor device characterized by having the conductive layer electrically connected to said reference potential electrode through opening of said 2nd insulating layer with the wrap in said 2nd insulating layer.

[Claim 2] The semiconductor device characterized by having further the protective coat to which opening of the part corresponding to the upper part of said external electrode terminal was carried out with the wrap in said conductive layer in a semiconductor device according to claim 1.

[Claim 3] The semiconductor device characterized by preparing the letter electrode of a projection on said external electrode terminal in a semiconductor device according to claim 1 or 2.

[Claim 4] The process which forms the 1st insulating layer on the principal plane of the semiconductor chip which has the reference potential electrode connected with an electrode at a reference potential where opening of the part corresponding to the upper part of said electrode and the part corresponding to the upper part of said reference potential electrode is carried out respectively, Wiring which connected with said electrode through

opening of said 1st insulating layer, and extended to up to said 1st insulating layer. The process which prepares respectively the external electrode terminal linked to said wiring on said 1st insulating layer, The process which forms the 2nd insulating layer which carried out opening of the part corresponding to the upper part of said reference potential electrode, and the part corresponding to the upper part of said external electrode terminal for said electrode and said wiring respectively with the wrap, The manufacture approach of the semiconductor device characterized by having the process which forms the conductive layer which connected said 2nd insulating layer to said reference potential electrode electrically through opening of said 2nd insulating layer with the wrap.

[Claim 5] The manufacture approach of the semiconductor device characterized by having further the process which forms the protective coat which carried out opening of the part corresponding to the upper part of said external electrode terminal for said conductive layer with the wrap in the manufacture approach of a semiconductor device according to claim 4.

[Claim 6] The manufacture approach of the semiconductor device characterized by preparing the letter electrode of a projection on said external electrode terminal in the manufacture approach of a semiconductor device according to claim 4 or 5.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] While this invention protects the integrated-circuit section containing semiconductor devices, such as a transistor, securing the electric connection to an external device and enabling higher-density mounting, it is related with the semiconductor device with little unnecessary radiation and its manufacture approach to the effect and the exterior by the noise from the outside.

[0002]

[Description of the Prior Art] In recent years, a miniaturization, densification, and improvement in the speed have come to be required from a semiconductor device with the miniaturization of electronic equipment, and advanced features. for this reason -- for example, a package called muBGA (micro ball grid array) (Patent Publication Heisei No. 504408 [06 to] official report) which LOC (lead-on chip), SON (small outline non lead), etc. were developed as a package for memory, or used the TAB tape is developed.

[0003] Hereafter, the conventional

semiconductor device called muBGA and its manufacture approach are explained, referring to drawing 5 . Drawing 5 is the sectional view showing the conventional semiconductor device called muBGA. In drawing 5 , the semiconductor chip with which 101 builds in semiconductor devices, such as a transistor, the wiring circuit sheet with which 102 was prepared on the semiconductor chip 101, the pliant low modulus-of-elasticity ingredient with which 103 intervenes between a semiconductor chip 101 and the wiring circuit sheet 102, the partial lead whose wiring circuit sheet 102 has 104, the electrode with which a semiconductor chip 101 has 105, and 106 are the electrodes of the wiring circuit sheet 102, and are an external electrode for connecting a semiconductor device and an external device. As shown in drawing 5 , the semiconductor device called muBGA has the structure where the wiring circuit sheet 102 was joined through the low modulus-of-elasticity ingredient 103 on the semiconductor chip 101, and the electrode 105 of a semiconductor chip 101 and the external electrode 106 of the wiring circuit sheet 102 are electrically connected through the partial lead 104.

[0004] Next, the manufacture approach of the conventional semiconductor device called muBGA is explained with reference to drawing 5 . First, the wiring circuit sheet 102 which has the partial lead 104 installed from the external electrode 106 and this external electrode 106 is laid through the low elastic-modulus ingredient 103 on a semiconductor chip 101. Next, in case it connects electrically by the "TAB" (tape automated bonding) activity, the partial lead 104 and an electrode 105 are electrically connected with the conventional thermocompression bonding technique or conventional ultrasonic-bonding technique usually used. The semiconductor device called muBGA was manufactured by the above approach.

[0005]

[Problem(s) to be Solved by the Invention] However, since a semiconductor chip 101 tended to be influenced by the noise component from the outside since the electrode 105 and the partial lead 104 had become the structure which is not covered electrically according to the above-mentioned conventional semiconductor device, and unnecessary radiation of semiconductor chip 101 self also became large, it had the fault of not being suitable for high-speed operation.

[0006] This invention aims at offering the semiconductor device which cannot be easily influenced of the noise component from the outside, and can reduce unnecessary radiation of the semiconductor device itself, and its manufacture approach by using the metal

wiring layer electrically connected to the reference potential electrode of a semiconductor chip as an electric shielding layer in view of the above-mentioned conventional technical problem.

[0007]

[Means for Solving the Problem] In order to attain this purpose, the semiconductor device concerning this invention The semiconductor chip with which the reference potential electrode connected with an electrode on a principal plane at a reference potential has been arranged, The 1st insulating layer to which it was prepared on the principal plane and opening of the part corresponding to the upper part of an electrode and the part corresponding to the upper part of a reference potential electrode was carried out respectively, Wiring which was connected to the electrode through opening of the 1st insulating layer, and extended to up to the 1st insulating layer, The external electrode terminal for connecting with wiring, being prepared on the 1st insulating layer, and delivering and receiving a signal between external instruments, It has the conductive layer electrically connected [insulating layer / 2nd insulating-layer / to which opening of part / of reference potential electrode / corresponding to the upper part / and part corresponding to the upper part of external electrode terminal was respectively carried out with wrap /, and / 2nd] to the reference potential electrode through opening of the 2nd insulating layer with the wrap in an electrode and wiring.

[0008] Since this prepared the conductive layer by which wiring and the electrode of a semiconductor chip were electrically connected with the reference potential electrode on the 2nd insulating layer of a wrap, it becomes the semiconductor device which cannot be easily influenced by the noise component from the outside, and cannot generate the unnecessary radiation from the semiconductor chip itself easily.

[0009] As for the semiconductor device of this invention, in here, it is desirable to have further the protective coat to which opening of the part corresponding to the upper part of an external electrode terminal was carried out with the wrap in the conductive layer. Thereby, since parts other than an external electrode terminal are covered with a protective coat, the open circuit and short circuit of wiring in parts other than an external electrode terminal are prevented, and it becomes the semiconductor device which has high dependability.

[0010] The semiconductor device of this invention is good also as having prepared the letter electrode of a projection on the external electrode terminal. A signal can be delivered [thereby,] and received much more certainly through the letter electrode of a projection between a

semiconductor device and an external instrument.

[0011] Moreover, the manufacture approach of the semiconductor device concerning this invention The process which forms the 1st insulating layer on the principal plane of the semiconductor chip which has the reference potential electrode connected with an electrode at a reference potential where opening of the part corresponding to the upper part of an electrode and the part corresponding to the upper part of a reference potential electrode is carried out respectively, Wiring which connected with the electrode through opening of the 1st insulating layer, and extended to up to the 1st insulating layer, The process which prepares the external electrode terminal linked to wiring respectively on the 1st insulating layer, The process which forms the 2nd insulating layer which carried out opening of the part corresponding to the upper part of a reference potential electrode, and the part corresponding to the upper part of an external electrode terminal for an electrode and wiring respectively with the wrap, It has the process which forms the conductive layer which connected the 2nd insulating layer to the reference potential electrode electrically through opening of the 2nd insulating layer with the wrap.

[0012] Since according to this approach this conductive layer is electrically connected with a reference potential electrode at the same time it forms a conductive layer on the 2nd insulating layer, the exclusive process which connects a conductive layer , and a reference potential electrode can be made unnecessary. Therefore, the semiconductor device which cannot be easily influenced by the noise component from the outside, and cannot generate the unnecessary radiation from the semiconductor chip itself easily due to a small man day can be manufactured.

[0013] As for the manufacture approach of the semiconductor device of this invention, in here, it is desirable to have further the process which forms the protective coat which carried out opening of the part corresponding to the upper part of an external electrode terminal for the conductive layer with the wrap. Thereby, the semiconductor device which has high dependability can be obtained by preventing an open circuit and short circuit of wiring by that of a wrap by the protective coat. [in / for parts other than an external electrode terminal / parts other than an external electrode terminal]

[0014] Moreover, the manufacture approach of the semiconductor device of this invention is good also as preparing the letter electrode of a projection on an external electrode terminal. Thereby, the semiconductor device a signal can be delivered and received much more

certainly through the letter electrode of a projection between a semiconductor device and an external instrument is obtained.

[0015]

[Embodiment of the Invention] The semiconductor device concerning this invention and its manufacture approach are explained referring to a drawing. It is the perspective view in which drawing 1's (a's)'s carrying out opening of a solder resist, an electric shielding metal layer, and the 2nd insulating layer for the outline of the semiconductor device concerning this invention partially, and removing and showing a part of metal ball, and drawing 1 (b) is a sectional view in the I-I line of drawing 1 (a).

[0016] The semiconductor chip with which 10 has semiconductor devices, such as a transistor, in drawing 1 (a) and (b), The usual electrode for 11A being prepared in the periphery section on the principal plane of a semiconductor chip 10, and delivering and receiving a signal between the exteriors, They are the reference potential electrode which 11B was prepared in the periphery section on the principal plane of a semiconductor chip 10, and was connected to the reference potential of a semiconductor chip 10, and the passivation film prepared by 12 usually exposing electrode 11A and reference potential electrode 11B on the principal plane of a semiconductor chip 10.

[0017] And the 1st insulating layer by which 20 was formed on the principal plane of a semiconductor chip 10, The 1st opening which 21 was formed in the 1st insulating layer 20, and usually exposed electrode 11A and reference potential electrode 11B, Metal wiring which 22A is usually connected to electrode 11A in the 1st opening 21, and is prolonged to up to the 1st insulating layer 20, Metal wiring which 22B is connected to reference potential electrode 11B in the 1st opening 21, and is prolonged to up to the 1st insulating layer 20, and 23A and 23B are the lands respectively formed in one on the 1st insulating layer 20 at the end of the metal wiring 22A and 22B.

[0018] Furthermore, the 2nd insulating layer formed by 24 exposing Lands 23A and 23B and metal wiring 22B on reference potential electrode 11B in the principal plane of a semiconductor chip 10, The 2nd opening formed by 25 exposing Lands 23A and 23B in the 2nd insulating layer 24, The 3rd opening formed by 26 exposing metal wiring 22B on reference potential electrode 11B in the 2nd insulating layer 24, The electric shielding metal layer which 27 was formed on the 2nd insulating layer 24, and was electrically connected with reference potential electrode 11B through metal wiring 22B in the 3rd opening 26, The solder resist formed by 28 exposing Lands 23A and 23B on the principal plane of a semiconductor chip 10 and 29

are the metal balls respectively joined on land 23A and 23B.

[0019] The electric shielding metal layer 27 formed so that the description of the semiconductor device of this invention might be on the 2nd insulating layer 24 and usual electrode 11A of a semiconductor chip 10 and metal wiring 22A might be covered here is connecting electrically as follows. That is, the electric shielding metal layer 27 is connected to land 23B to which it corresponds of the lands which are external electrode terminals, respectively while connecting with the reference potential of a semiconductor chip 10 through metal wiring 22B and reference potential electrode 11B one by one. Furthermore, it means that the electric shielding metal layer 27 was connected to the reference potential of an external instrument equal to the reference potential of a semiconductor chip 10 through metal wiring 22B, land 23B, and the metal ball 29 one by one after a semiconductor device was mounted in an external instrument. Therefore, the semiconductor device which cannot be easily influenced by the noise component from the outside, and can reduce the unnecessary radiation from semiconductor chip 10 self by the electric shielding metal layer 27 which has potential equal to the reference potential of a semiconductor device is realized.

[0020] Hereafter, the manufacture approach of the semiconductor device concerning this invention is explained, referring to drawing 2 - drawing 4. Drawing 2 (a) - (d) is the sectional view showing each process to plating resist pattern formation among the manufacture approaches concerning this invention, respectively.

[0021] First, as shown in drawing 2 (a), the photosensitive insulating material 30 is applied to the thickness of about 100 micrometers on the principal plane of the semiconductor chip 10 with which electrode 11A and reference potential electrode 11B were usually exposed, and the passivation film 12 was formed. Here, as a photosensitive insulating material 30, what is necessary is just the polymer which has the photosensitivity and insulation of ester bond mold polyimide, acrylate system epoxy, etc., for example.

[0022] Next, as shown in drawing 2 (b), by performing desiccation, exposure, and development one by one, patterning of the photosensitive insulating material 30 is carried out, and the 1st insulating layer 20 which has the 1st opening 21 which usually exposes electrode 11A and reference potential electrode 11B is formed.

[0023] Next, as shown in drawing 2 (c), on the whole surface of the principal plane of a semiconductor chip 10, the thin film metal layer 31 which consists of Ti/Cu is formed in the thickness of about 0.05 micrometers with a vacuum deposition

method. Here, it may replace with a vacuum deposition method and a nonelectrolytic plating method, the sputtering method, or a CVD method may be used.

[0024] Next, as shown in drawing 2 (d), a negative-mold photosensitivity resist is applied and exposed on the thin film metal layer 31, and it stiffens, the parts, i.e., the sensitization section, other than the pattern section of the request in a finishing product. After that, the plating resist pattern 32 is formed by removing, desired pattern section, i.e., non-exposed section. In addition, although the negative-mold photosensitivity resist was used in order to form the plating resist pattern 32, a positive type photosensitivity resist may be used here. In this case, the photo mask with which black and white were reversed will be used in the case of exposure.

[0025] Drawing 3 (a) - (d) is the sectional view showing each process from the thick-film metal stratification to the 2nd insulating stratification among the manufacture approaches concerning this invention, respectively.

[0026] It is the process shown in drawing 2 (d), next as shown in drawing 3 (a), the thick-film metal layer 33 is alternatively formed by the electrolysis galvanizing method on thin film metal layers 31 other than the part in which the plating resist pattern 32 was formed. Here, the thick-film metal layer 33 is formed in the thickness of about 20 micrometers using Cu.

[0027] Next, as shown in drawing 3 (b), the plating resist pattern 32 is fused and removed.

[0028] Next, as shown in drawing 3 (c), after carrying out overall etching of the Cu using the etching reagent which fuses the thin film metal layer 31 and the thick-film metal layer 33, for example, a cupric-chloride solution, an EDTA solution is used and overall etching of Ti is carried out. This precedes and removes the thin film metal layer 31 which has thickness smaller than the thick-film metal layer 33. Therefore, in a desired field, the metal wiring 22A and 22B and Lands 23A and 23B which consist of a thick-film metal layer 33 and a thin film metal layer 31, respectively are formed. Here, after removing the plating resist pattern 32, a photolithography technique may be used and the thick-film metal layer 33 may be protected by forming etching resist on the pattern for which it asks.

[0029] Next, as shown in drawing 3 (d), after applying a photosensitive insulating material all over the principal plane of a semiconductor chip 10, the 2nd insulating layer 24 is formed like the process which forms the 1st insulating layer 20 shown in drawing 2 (b). By the 2nd formed insulating layer 24, on the principal plane of a semiconductor chip 10, Lands 23A and 23B and metal wiring 22B on

reference potential electrode 11B are exposed, and the remaining part is protected. In this case, the 2nd opening 25 will be formed in the part of Lands 23A and 23B, and the 3rd opening 26 will be formed in the part of metal wiring 22B on reference potential electrode 11B.

[0030] Drawing 4 (a) - (d) is the sectional view showing each process from the electric shielding metal stratification to metal ball junction among the manufacture approaches concerning this invention, respectively.

[0031] It is the process shown in drawing 3 (d), next as shown in drawing 4 (a), on the whole surface of the principal plane of a semiconductor chip 10, the electric shielding metal layer 27 which consists of Cu is formed in the thickness of about 0.5 micrometers with a vacuum deposition method. The electric shielding metal layer 27 is electrically connected to Lands 23A and 23B by this in the 2nd opening 25 while connecting with reference potential electrode 11B electrically through metal wiring 22B in the 3rd opening 26 formed in the 2nd insulating layer 24, respectively. Here, it may replace with a vacuum deposition method and a nonelectrolytic plating method, the sputtering method, or a CVD method may be used.

[0032] Next, as shown in drawing 4 (b), the etching resist pattern 34 is formed with a photolithography technique to fields other than land 23A and 23B on the electric shielding metal layer 27, and the electric shielding metal layer 27 which is not covered with the etching resist pattern 34 is etched for example, using a cupric-chloride solution. This removes the electric shielding metal layer 27 on the 2nd opening 25, i.e., the part which the electric shielding metal layer 27 has connected with Lands 23A and 23B too hastily. In this case, in order to remove the short-circuited part certainly, as it has bigger opening than the 2nd opening 25 in which the 2nd insulating layer 24 has the etching resist pattern 34, it is formed.

[0033] Next, as shown in drawing 4 (c), after removing the etching resist pattern 34, a solder resist 28 is formed to fields other than land 23A and 23B on the principal plane of a semiconductor chip 10. By this, while exposing only Lands 23A and 23B, the electric shielding metal layer 27 is protected.

[0034] Next, as shown in drawing 4 (d), after laying the metal ball 29 on land 23A and 23B, the metal ball 29 and Lands 23A and 23B are fused, and it joins. Here, as an ingredient of the metal ball 29, metals by which solder plating was carried out, such as solder, copper, and nickel, are used.

[0035] As explained above, according to the manufacture approach of the semiconductor device concerning this invention, the electric shielding metal layer 27 is formed in the front face of the

2nd insulating layer 24 prepared as covered usual electrode 11A of a semiconductor chip 10, and metal wiring 22A, and the electric shielding metal layer 27 and reference potential electrode 11B of a semiconductor chip 10 are electrically connected to coincidence in the 3rd opening 26 formed in the 2nd insulating layer 24. By this, the exclusive process for connecting electrically the electric shielding metal layer 27 and reference potential electrode 11B can be made unnecessary. Therefore, processes are reduced and the semiconductor device which cannot be easily influenced by the noise component from the outside, and can reduce the unnecessary radiation from semiconductor chip 10 self by the electric shielding metal layer 27 can be manufactured by low cost.

[0036] In addition, in the above explanation, although the ingredient liquefied as a photosensitive insulating material 30 was applied, it may replace with this and the ingredient which is beforehand formed in the shape of a film, and has photosensitivity and insulation may be used. In this case, by sticking the photosensitive film-like insulating material 30 on the principal plane of a semiconductor chip 10, uniting it, and exposing and developing it, the 1st opening 21 is formed in the 1st insulating layer 20, and usual electrode 11A of a semiconductor chip 10 and reference potential electrode 11B are exposed.

[0037] Moreover, it may replace with the photosensitive insulating material 30, and the insulating material which does not have photosensitivity may be used. In this case, what is necessary is just to expose usual electrode 11A of a semiconductor chip 10, and reference potential electrode 11B by mechanical processing of laser, the plasma, sandblasting, etc., or chemical processing of etching etc.

[0038] Moreover, the shielding layer which consists of conductive resin which replaces with the electric shielding metal layer 27 which consists of Cu, for example, contains particles, such as Cu and Ag, may be used. In this case, a shielding layer can be formed by applying conductive resin on the 2nd insulating layer 24 using print processes, a spin coat method, etc.

[0039] Furthermore, although the case where electrode 11A and reference potential electrode 11B were usually prepared in the periphery section on the principal plane of a semiconductor chip 10 was explained Not only this but when electrode 11A and reference potential electrode 11B are usually prepared in the center section on the principal plane of a semiconductor chip 10 and the 1st opening 21 is formed in the 1st insulating layer 20 in the center section, it cannot be overemphasized that the semiconductor device and its manufacture approach of this invention are applicable.

[0040]

[Effect of the Invention] Since the electric shielding metal layer formed so that it might be on the 2nd insulating layer and the usual electrode of a semiconductor chip and metal wiring might be covered is electrically connected with the reference electrode of a semiconductor chip according to the semiconductor device of this invention, it is hard to be influenced by the noise component from the outside, and the unnecessary radiation from a semiconductor chip can be reduced.

[0041] Moreover, according to the manufacture approach of the semiconductor device of this invention, the exclusive process for connecting electrically an electric shielding metal layer and a reference potential electrode can be made unnecessary, and the semiconductor device of this invention can be manufactured by the small man day.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the perspective view showing the outline of the semiconductor device which (a) carries out opening of some components partially, and removes some another components, and is applied to this invention, and (b) is a sectional view in the I-I line of (a).

[Drawing 2] (a) - (d) is the sectional view showing each process to plating resist pattern formation among the manufacture approaches concerning this invention, respectively.

[Drawing 3] (a) - (d) is the sectional view showing each process from the thick-film metal stratification to the 2nd insulating stratification among the manufacture approaches concerning this invention, respectively.

[Drawing 4] (a) - (d) is the sectional view showing each process from the electric shielding metal stratification to metal ball junction among the manufacture approaches concerning this invention, respectively.

[Drawing 5] It is the sectional view showing the conventional semiconductor device called muBGA.

[Description of Notations]

10 Semiconductor Chip

11A Usually, an electrode

11B Reference potential electrode

12 Passivation Film

20 1st Insulating Layer

21 1st Opening

22A, 22B Metal wiring (wiring)

23A, 23B Land (external electrode terminal)

24 2nd Insulating Layer

25 2nd Opening

26 3rd Opening

27 Electric Shielding Metal Layer (Conductive Layer)

28 Solder Resist (Protective Coat)

29 Metal Ball (Letter Electrode of Projection)

30 Photosensitive Insulating Material

31 Thin Film Metal Layer

32 Plating Resist Pattern

33 Thick-Film Metal Layer

34 Etching Resist Pattern

[Translation done.]